QUAD TWO-INPUT NOR GATE

4001
276-2401

GENERAL DESCRIPTION

The 4001 quad 2-Input NOR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

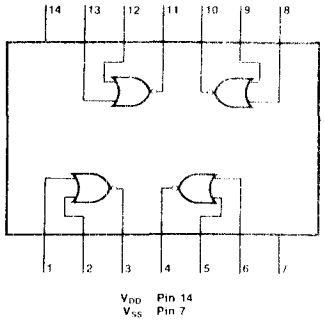
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq \{V_{in} \text{ or } V_{out}\} \leq V_{DD}$.

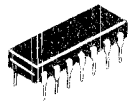
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FEATURES

- Quiescent Current = 0.5 nA typ/pkg@ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 16 Vdc
- Single Supply Operation—Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout

PIN CONNECTION





ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS})

DC Supply Voltage	-0.5 to +16 Vdc
Input Voltage, All Inputs	-0.5 to V_{DD} +0.5 Vdc
DC Current Drain per Pin	10 mAdc
Operating Temperature Range	-40 to 85°C
Storage Temperature Range	-65 to +150°C

QUAD TWO-INPUT NAND GATE

4011
276-2411

GENERAL DESCRIPTION

The 4011 is constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

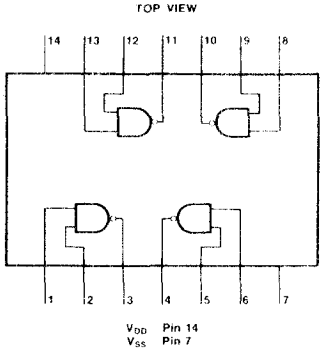
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq \{V_{in} \text{ or } V_{out}\} \leq V_{DD}$

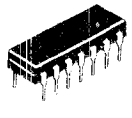
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FEATURES

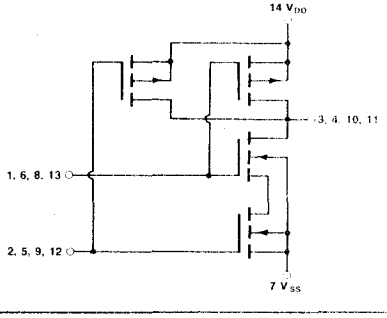
- Quiescent Current = 0.5 nA typ/pkg@ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 16 Vdc
- Double Diode Protection on All Inputs

PIN CONNECTION





CIRCUIT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS})

DC Supply	-0.5 to +16 Vdc
Input Voltage, All Inputs	-0.5 to V_{DD} +0.5 Vdc
DC Current Drain per Pin	10 mAdc
Operating Temperature Range	-40 to +85°C
Storage Temperature Range	-65 to +150°C